Code.No: RR320405 | RR | SET-1

III B.TECH – II SEM EXAMINATIONS, DECEMBER - 2010
VLSI DESIGN
(COMMON TO ECE & ETM)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1.a) Explain about the Electrical characteristics of MOSFET devices.
b) Explain in detail about the BICMOS process. [8+8]

2.a) Compare Bipolar and CMOS processes.
b) Explain the terms Inverter delays, propagation delays, and wiring capacitance. [8+8]

3. Give the notations used in stuck diagram for CMOS inverter, giving explanation. [16]

4.a) Explain the principle and Architecture of FPGA.
b) Explain about the applications of PLAs. [8+8]

5.a) Draw the functional block of CPLD and explain the same.
b) What are the various design verification tools used in VLSI design? Explain. [8 +8]

6. Explain about the following terms pertaining to VLSI simulation;
(i) Behavioral simulation
(ii) Functional simulation
(iii) Gate-level simulation
(iv) Switch-level simulation
(v) Circuit-level simulation. [16]

7. Draw the sketch and explain about the Twin-Tub process for CMOS fabrication. [16]

8. Write short notes on any **TWO** of the following:
(i) IC packaging Techniques
(ii) Ion-Implantation
(iii) VLSI design flow. [16]

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Code.No: RR320405 | RR | SET-2

III B.TECH – II SEM EXAMINATIONS, DECEMBER - 2010
VLSI DESIGN
(COMMON TO ECE & ETM)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1. Give the notations used in stuck diagram for CMOS inverter, giving explanation. [16]

2.a) Explain the principle and Architecture of FPGA.
b) Explain about the applications of PLAs. [8+8]

3.a) Draw the functional block of CPLD and explain the same.
b) What are the various design verification tools used in VLSI design? Explain. [8 +8]

4. Explain about the following terms pertaining to VLSI simulation;
(i) Behavioral simulation
(ii) Functional simulation
(iii) Gate-level simulation
(iv) Switch-level simulation
(v) Circuit-level simulation. [16]

5. Draw the sketch and explain about the Twin-Tub process for CMOS fabrication. [16]

6. Write short notes on any **TWO** of the following:
(i) IC packaging Techniques
(ii) Ion-Implantation
(iii) VLSI design flow. [16]

7.a) Explain about the Electrical characteristics of MOSFET devices.
b) Explain in detail about the BICMOS process. [8+8]

8.a) Compare Bipolar and CMOS processes.
b) Explain the terms Inverter delays, propagation delays, and wiring capacitance. [8+8]

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Code.No: RR320405 | RR | SET-3

III B.TECH – II SEM EXAMINATIONS, DECEMBER - 2010
VLSI DESIGN
(COMMON TO ECE & ETM)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1.a) Draw the functional block of CPLD and explain the same.
b) What are the various design verification tools used in VLSI design? Explain. [8 +8]

2. Explain about the following terms pertaining to VLSI simulation;
(i) Behavioral simulation
(ii) Functional simulation
(iii) Gate-level simulation
(iv) Switch-level simulation
(v) Circuit-level simulation. [16]

3. Draw the sketch and explain about the Twin-Tub process for CMOS fabrication. [16]

4. Write short notes on any **TWO** of the following:
(i) IC packaging Techniques
(ii) Ion-Implantation
(iii) VLSI design flow. [16]

5.a) Explain about the Electrical characteristics of MOSFET devices.
b) Explain in detail about the BICMOS process. [8+8]

6.a) Compare Bipolar and CMOS processes.
b) Explain the terms Inverter delays, propagation delays, and wiring capacitance. [8+8]

7. Give the notations used in stuck diagram for CMOS inverter, giving explanation. [16]

8.a) Explain the principle and Architecture of FPGA.
b) Explain about the applications of PLAs. [8+8]

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Code.No: RR320405 | RR | SET-4

III B.TECH – II SEM EXAMINATIONS, DECEMBER - 2010
VLSI DESIGN
(COMMON TO ECE & ETM)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1. Draw the sketch and explain about the Twin-Tub process for CMOS fabrication. [16]

2. Write short notes on any **TWO** of the following:
   (i) IC packaging Techniques
   (ii) Ion-Implantation
   (iii) VLSI design flow. [16]

3.a) Explain about the Electrical characteristics of MOSFET devices.
b) Explain in detail about the BICMOS process. [8+8]

4.a) Compare Bipolar and CMOS processes.
b) Explain the terms Inverter delays, propagation delays, and wiring capacitance. [8+8]

5. Give the notations used in stuck diagram for CMOS inverter, giving explanation. [16]

6.a) Explain the principle and Architecture of FPGA.
b) Explain about the applications of PLAs. [8+8]

7.a) Draw the functional block of CPLD and explain the same.
b) What are the various design verification tools used in VLSI design? Explain. [8 +8]

8. Explain about the following terms pertaining to VLSI simulation;
   (i) Behavioral simulation
   (ii) Functional simulation
   (iii) Gate-level simulation
   (iv) Switch-level simulation
   (v) Circuit-level simulation. [16]

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